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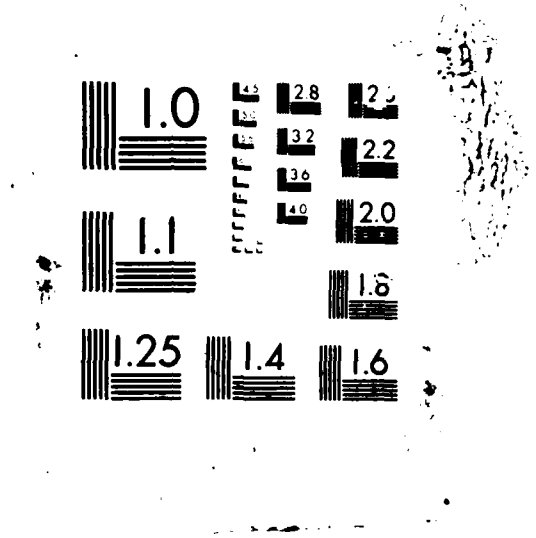
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REPORT SD-TR-86-67

AD-A176 234

SEU Tolerance of McDonnell Douglas' CMOS/SOS High Performance 3 Chip Implementation of MIL-STD-1750A Instruction Set

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30 September 1986

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Los Angeles Air Force Station
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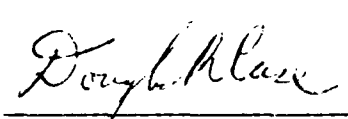
This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-85-C-0086 with the Space Division, P.O. Box 92960, Worldway Postal Center, Los Angeles, CA 90009-2960. It was reviewed and approved for The Aerospace Corporation by H. R. Rugge, Director, Space Sciences Laboratory.

Capt Douglas R. Case, SD/YCM, was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.



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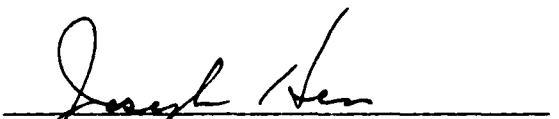

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*
A single event upset (SEU) experiment was conducted on the control unit (CU) chip of McDonnell Douglas' 1750A microprocessor (called the MD281), as a joint effort of McDonnell Douglas Corporation and The Aerospace Corporation at the 88 inch cyclotron, Lawrence Berkeley Laboratory. No upset was detected using a 140 MeV krypton beam. Test results, geometry, and process parameters are used to predict a failure threshold and an upset rate.

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CONTENTS

I. INTRODUCTION

McDonnell Douglas Astronautics Company, in cooperation with The Aerospace Corporation, tested the control unit (CU) chip of the MD281 CMOS/SOS chip set for high energy particle radiation (HEPR) effect also referred to as single event upset (SEU). The test, which was sponsored by the Air Force Space Technology Center (AFSTC), Albuquerque, NM, was conducted in October 1984 at the 88" cyclotron, Lawrence Berkeley Laboratory, Berkeley, Ca. The MD281 is the highest performance 1750A microprocessor in existence today. It is also radiation hard by circuit design. The throughput rate is 940 kips (dais) or 1.6 mips without floating point operations (dis). The CU chip is a VLSI chip with over 65,000 FETs divided between: a 10,000 FET microcode sequencer, an 8 × 16-bit register section, and a 45,000 FET microcode store (1.024 × 40-bit storage capacity). The chip is fabricated using MDC's 4 μm, self-aligned polysilicon gate, ion implanted source/drain CMOS/SOS radiation hard process, MDC's CSII process. The chip is hardened by circuit design, choice of processing technology (silicon-on-sapphire), and by special IC processing steps to improve radiation tolerance (1,2,3).

II. SEU EXPERIMENT

The device under test (DUT) was exercised to stress four vulnerable areas and observe failure if it occurs by comparing the acquired data from the device to known reference data recorded in the test chamber when the HEPR source is turned off. The vulnerable areas are: (1) the register section which has the vulnerability of static RAM cells, (2) the bit lines of the microcode store, which are very long precharged lines and can exhibit the types of problems seen in dynamic logic, (3) the sense amplifiers of the microcode store, which can be very sensitive to noise-like disturbances caused by the radiation, and (4) the random logic of the sequencer state machine, which if upset can cause the sequencer to go to unknown states with unpredictable execution sequences.

Because of the high speed of the processor [uses a 30 MHz oscillator clock to complete a microinstruction cycle in 167 nanoseconds (5 clock period)], we used a Tektronix Digital Analysis System (DAS) 9100 as the test pattern generator. The DAS 9100 is capable of generating test patterns at rates from almost dc to 100 MHz. We used the 40 MHz pattern generator version. The DAS was located with the DUT in the shielded test room less than 6 ft from the canister that holds the DUT. The control of the DAS 9100, the acquisition of test data, and the comparison were done remotely using a Hewlett-Packard (HP) 9836 desk-top computer. Data were communicated over the IEEE 488-1975 byte-wide standard bus. The remote control and data acquisition programs, which are written in PASCAL, can be used for other radiation tests using the Tektronix DAS 9100 tester. Test data were logged into a 5-1/4-in. floppy disk for archieval purposes. Other data kept included information to identify each run of the test, the number of errors, and the time elapsed. The same data can be sent to the CRT or to a hard copy device immediately or off-line.

III. TEST RESULTS

Since we know apriori (5) that 4 μm CMOS/SOS is inherently hard to SEU, the beam species used were krypton (4). The energy level used in this experiment was 140 MeV which was the highest attainable at this facility. We made 21 runs with different particle fluences up to 107 particles/cm^2,and different beam incidence angles from 0 to 75°. No upset was observed in any of these runs. To make sure that the test setup was capable of detecting upsets, we forced the part to fail by lifting pins from the socket which simulates hard errors. We also applied a burst of visible light using an electronic camera flash which simulates soft errors (upsets). We were able to record upsets using both methods in and out of the shielded test room. To make sure that the enclosing of the DUT was not a factor, we simulated the hard and soft errors in and out of the canister.

The geometry and doping information for the CSII process was used to compute the critical parameters for SEU, namely; critical length, critical area, critical volume, and critical charge. The theoretical computations indicate that the critical charge cannot be less than 0.33 pico Coulomb for a minimum device used in this design. However, in practice a minimum device is never used by itself as a load. More typically, three times the minimum is used for a minimum load and this indicates a minimum critical charge of 0.99 pico Coulomb. For the register section, the minimum critical charge was computed to be not less than 0.48 pico Coulomb. For the ROM section, the minimum critical charge is greater than 1.0 pico Coulomb due to the big loads imposed by layout, ROM size, and layout density. The critical charge computation was done for 5 V supply which is the voltage used to operate the CU during the SEU experiment. Since the part was designed to operate at 12 V we can safely assume that the actual critical charge is more than double the above mentioned figures.

The analysis of test data indicates that the minimum linear energy transport (LET) threshold is greater than 120 MeV/mg/cm^2 which is equivalent to 1.2 pico Coulomb/micron. This translates to a critical charge for upset

greater than 0.7 pico Coulomb using 0.6 μm as the critical length. Since the part was running at 5 V during the test, but the voltage level for actual use in space applications is 12 V, we can safely predict that the minimum LET threshold for the part operating at specified supply voltage is greater than 288 MeV/mg/cm^2, which is equivalent to 2.88 pico Coulomb/micron. This translates to a critical charge for upset greater than 1.68 pico Coulomb at 12 V (for silicon on insulator (sapphire), one does not have to worry about the funneling effect in computing critical charge). Applying the Crier Code to the test data, we predict that the upset rate for the CU chip (operating at 5 V) will be lower than 9×10^{-8} upset/day.

IV. CONCLUSIONS

In conclusion, we found the CU chip of the MD281 chip set extremely resistant to SEU even when operating with 5 V supply. This VLSI part is representative of the geometry and doping level of the other chips in the MD281 chip set. This leads us to believe that the the other chips in the chip set have the same SEU tolerance level. By combining the incomplete results of an expensive SEU test with the data on the geometry of the devices and the CSII process parameters, we were able to estimate a minimum LET threshold and an upper bound on the upset rate for the CU chip. These estimates are applicable as well to the other chips in the MD281 chip set.

V. RECOMMENDATIONS

It is recommended that this experiment be repeated using a higher Z material (e.g., gold) and a higher energy level to experimentally determine the exact failure threshold of the CU chip. It is also recommended that the individual chips in the MD281 chip set be tested to obtain conclusive data on the SEU tolerance.

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LABORATORY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security projects, specializing in advanced military space systems. Providing research support, the corporation's Laboratory Operations conducts experimental and theoretical investigations that focus on the application of scientific and technical advances to such systems. Vital to the success of these investigations is the technical staff's wide-ranging expertise and its ability to stay current with new developments. This expertise is enhanced by a research program aimed at dealing with the many problems associated with rapidly evolving space systems. Contributing their capabilities to the research effort are these individual laboratories:

Aerophysics Laboratory: Launch vehicle and reentry fluid mechanics, heat transfer and flight dynamics; chemical and electric propulsion, propellant chemistry, chemical dynamics, environmental chemistry, trace detection; spacecraft structural mechanics, contamination, thermal and structural control, high temperature thermomechanics, gas kinetics and radiation; cw and pulsed chemical and excimer laser development including chemical kinetics, spectroscopy, optical resonators, beam control, atmospheric propagation, laser effects and countermeasures.

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Materials Sciences Laboratory: Development of new materials: metals, alloys, ceramics, polymers and their composites, and new forms of carbon; nondestructive evaluation, component failure analysis and reliability; fracture mechanics and stress corrosion; analysis and evaluation of materials at cryogenic and elevated temperatures as well as in space and enemy-induced environments.

Space Sciences Laboratory: Magnetospheric, auroral and cosmic ray physics, wave-particle interactions, magnetospheric plasma waves; atmospheric and ionospheric physics, density and composition of the upper atmosphere, remote sensing using atmospheric radiation; solar physics, infrared astronomy, infrared signature analysis; effects of solar activity, magnetic storms and nuclear explosions on the earth's atmosphere, ionosphere and magnetosphere; effects of electromagnetic and particulate radiations on space systems; space instrumentation.

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